What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for refreshing memory cells, comprising:

determining that a refresh of said memory cells is required;

determining that a data access is desired; and

initiating said refresh at a predetermined time without delaying said data access.

2. The method of claim 1, wherein said act of determining that a data access is desired comprises determining that a data access command has been applied to a command/address bus at a predetermined time slot.

3. The method of claim 1, wherein said act of initiating comprises initiating said refresh within a predetermined time slot of a command/address bus.

4. The method of claim 2 further comprising determining whether said data access command conflicts with said refresh.

5. The method of claim 4 further comprising:

determining that said data access command does not conflict with said refresh; and

performing said refresh.

6. The method of claim 4 further comprising:

determining that said data access command does conflict with said refresh;

completing said conflicting data access;

waiting for a next available time slot upon which said refresh may be initiated; and

initiating said refresh upon reaching said next available time slot without conflicting with a second data access.

7. The method of claim 6 further comprising determining whether a second data access command has been applied to said command/address bus at said next available time slot.

8. The method of claim 7 further comprising:

determining that a second data access command has been applied to said command/address bus at said predetermined time slot; and

determining whether said second data access command conflicts with said refresh.

9. The method of claim 8 further comprising:

determining that said second data access command does not conflict with said refresh; and

performing said refresh.

10. The method of claim 8 further comprising:

determining that said second data access command does conflict with said refresh;

completing said second conflicting data access;

waiting for a next available time slot upon which said refresh may be initiated; and

initiating said refresh upon reaching said next available time slot without conflicting with a third data access.

11. The method of claim 10 further comprising:

satisfying said second data access command by having said data access satisfied with a memory source other than said memory cells such that said memory cells can be refreshed; and

performing said refresh on said memory cells.

12. The method of claim 11, wherein said act of satisfying comprises satisfying said second data access command by having said data access satisfied with a static random access memory cache.

13. A system for refreshing memory cells of a dynamic random access memory (DRAM) comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

14. The system of claim 13, wherein said communication link comprises a command/address bus.

15. The system of claim 13 further comprising a memory source other than said memory cells such that said controller operates said DRAM such that said conflicting data access command is satisfied with said memory source other than said memory cells and wherein said memory cells may be refreshed.

16. The system of claim 15, wherein said memory source other than said memory cells comprises a static random access memory (SRAM) cache.

17. The system of claim 13, wherein said controller comprises a refresh controller.

18. The system of claim 13 further comprising:

a counter for counting clock cycles of a dynamic random access memory (DRAM) input clock, wherein at least some of said clock cycles define said predetermined time.

19. The system of claim 13, wherein said predetermined time is defined by receiving a predetermined edge of a data access command.

20. The system of claim 19, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.

21. The system of claim 20, wherein said DRAM input clock has a frequency of approximately 300 MHz.

22. The system of claim 13, wherein said communication link comprises a link for communicating read and/or write commands to said memory array.

23. A memory device, comprising:

a memory controller configured to operate said memory device to:

determine that a refresh of said memory cells is required;

determine that a data access is desired; and

initiate said refresh at a predetermined time without delaying said data access.

24. The memory device of claim 23, wherein said memory controller operates said memory device to determine that a data access command has been applied to a command/address bus at a predetermined time slot.

25. The memory device of claim 23, wherein said memory controller operates said memory device to initiate said refresh within a predetermined time slot of a command/address bus.

26. The memory device of claim 24, wherein said memory controller further operates said memory device to determine whether said data access command conflicts with said refresh.

27. The memory device of claim 26, wherein said memory controller further operates said memory device to:

determine that said data access command does not conflict with said refresh; and

perform said refresh.

28. The memory device of claim 26, wherein said memory controller further operates said memory device to:

determine that said data access command does conflict with said refresh;

complete said conflicting data access;

wait for a next available time slot upon which said refresh may be initiated; and

initiate said refresh upon reaching said next available time slot without conflicting with a second data access.

29. The memory device of claim 28, wherein said memory controller further operates said memory device to determine whether a second data access command has been applied to said command/address bus at said next available time slot.

30. The memory device of claim 29, wherein said memory controller further operates said memory device to:

determine that a second data access command has been applied to said command/address bus at said predetermined time slot; and

determine whether said second data access command conflicts with said refresh.

31. The memory device of claim 30, wherein said memory controller further operates said memory device to:

determine that said second data access command does not conflict with said refresh; and

perform said refresh.

32. The memory device of claim 30, wherein said memory controller further operates said memory device to:

determine that said second data access command does conflict with said refresh;

complete said second conflicting data access;

wait for a next available time slot upon which said refresh may be initiated; and

initiate said refresh upon reaching said next available time slot without conflicting with a third data access.

33. The memory device of claim 32, wherein said memory controller further operates said memory device to:

satisfy said second data access command by having said data access satisfied with a memory source other than said memory cells such that said memory cells can be refreshed; and

perform said refresh on said memory cells.

34. The memory device of claim 33, wherein said memory controller operates said memory device such that said act of satisfying comprises satisfying said second data access command by having said data access satisfied with a static random access memory cache.

35. An integrated circuit semiconductor device containing a system for refreshing memory cells of a dynamic random access memory (DRAM), said integrated circuit semiconductor device comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

36. The integrated circuit device of claim 35, wherein said communication link comprises a command/address bus.

37. The integrated circuit device of claim 35, wherein said system further comprises a memory source other than said memory cells such that upon

said controller determining that data stored in at least some of said memory cells is in danger of being lost as a result of not being refreshed, said controller operates said DRAM such that said conflicting data access command is satisfied with said memory source other than said memory cells and wherein said memory cells may be refreshed.

38. The integrated circuit device of claim 37, wherein said memory source other than said memory cells comprises a static random access memory (SRAM) cache.

39. The integrated circuit device of claim 35, wherein said controller comprises a refresh controller.

40. The integrated circuit device of claim 35, wherein said system further comprises:

a counter for counting clock cycles of a dynamic random access memory (DRAM) input clock, wherein at least some of said clock cycles correspond to said predetermined time.

41. The integrated circuit device of claim 35, wherein said predetermined time is defined by receiving a predetermined edge of a data access command.

42. The integrated circuit device of claim 41, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.

43. The integrated circuit device of claim 42, wherein said dynamic random access memory (DRAM) input clock has a frequency of approximately 300 MHz.

44. The integrated circuit device of claim 35, wherein said communication link comprises a link for communicating read and/or write commands to said memory array.

45. A processor-based system, comprising:

a processor; and

a dynamic random access memory (DRAM) coupled to said processor, said dynamic random access memory having a system for refreshing memory cells in said dynamic random access memory, said system comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

46. The processor-based system of claim 45, wherein said communication link comprises a command/address bus.

47. The processor-based system of claim 45, wherein said system for refreshing memory cells further comprises a memory source other than said memory cells such that said controller operates said DRAM such that said conflicting data access command is satisfied with said memory source other than said memory cells and wherein said memory cells may be refreshed.

48. The processor-based system of claim 47, wherein said memory source other than said memory cells comprises a static random access memory (SRAM) cache.

49. The processor-based system of claim 45, wherein said controller comprises a refresh controller.

50. The processor-based system of claim 45, wherein said system for refreshing memory cells further comprises:

a counter for counting clock cycles of a dynamic random access memory (DRAM) input clock, wherein at least some of said clock cycles define said predetermined time.

51. The processor-based system of claim 45, wherein said predetermined time is defined by receiving a predetermined edge of a data access command.

52. The processor-based system of claim 45, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.

53. The processor-based system of claim 52, wherein said DRAM input clock has a frequency of approximately 300 MHz.

54. The processor-based system of claim 45, wherein said communication link comprises a link for communicating read and/or write commands to said memory array.